

## Abstract:

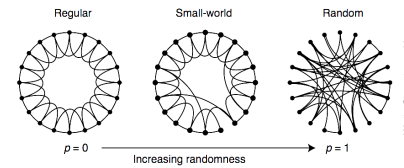
- **Goal:** investigate the properties of an irregular, abstract, yet physically plausible **small-world interconnect fabric for self-assembled nanoscale electronics**, inspired by modern network-on-chip (NoC) paradigms [2].
- We vary the framework's key parameters, such as the connectivity, the number of switch blocks, the number of virtual channels, the routing strategy, and the distribution of long- and short-range connections.
- We measure the network's **transport characteristics**, the robustness against failures, and solve toy problems.
- Is computation in **irregular and imperfect assemblies** a promising new computing paradigm for nanoscale electronics?
- **Yes**, better transport characteristics, more **robust**, **physically plausible**, and **fabrication friendly** [1].

## Introduction and motivation:

- Today, interconnects are more important than transistors [3].
- Current ad hoc interconnect technology is not suitable (global signals, delays, scalability) for self-assembled Avogadro-scale nanoscale electronics [3].
- We argue that **radically new approaches** potentially offer better performance for a lower price.
- We need physically plausible and fabrication friendly approaches.
- Nanoscale electronics and novel fabrication technologies bear unique opportunities for **self-assembling Avogadro-scale component systems in a largely random manner**, which would likely lower fabrication costs significantly compared to a definite ad hoc assembly [1].

## Complex networks:

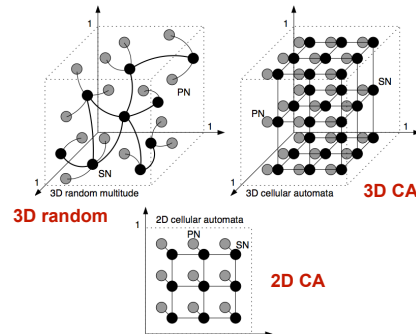
- Small-world networks have a short average path length.
- A **regular topology** is easy to build (local connections), but has rather poor transport characteristics.
- A **random network** is not physically plausible (uniform connection probability, independent of distance).
- **Small-world nets with a power-law distribution of the connection lengths** are physically plausible and have great transport characteristics [4,5].



## The framework:

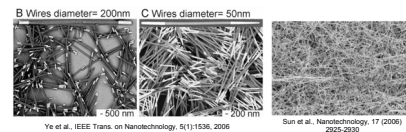
- Compare design and performance trade-offs of 2D and 3D regular with random small-world topologies [1].
- Network-on-chip (NoC) approach [2]:
  - programmable **computing/processing nodes** (PNs)
  - **switch nodes** (SNs), and
  - bi-directional point-to-point interconnects.
- SNs only route packets, PNs can do computation, every PN is connected to the nearest SN.
- SNs can have a rich interconnect fabric among themselves and do **random** or **shortest-path** routing.
- **Random multitude** (RM):
  - PNs and SNs are randomly arranged in space
  - **Power law** ( $l^{-\alpha}$ ) and **Gaussian** connection distribution as a function of the Euclidian distance.
  - **Lots of local, few "global" connections**, depending on the Euclidian distance
  - $\alpha = 0$ : original Watts-Strogatz topology

## Comparing different interconnects:



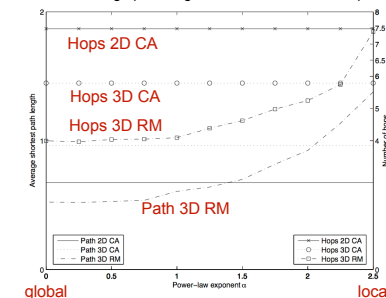
## Fabrication by self-assembly:

- We imagine a hybrid approach first:
  - Nodes: traditional silicon
  - Interconnections: self-assembled nanowires or nanotubes
- Wires can be easily self-assembled in huge, i.e., Avogadro-scale quantities.
- It is easier to establish random and imperfect interconnections than to come up with a perfect alignment.
- Power-law distributions occur very frequently in Nature (optimal transport under restricted resources).
- Future work: realistic wire-growth models are needed.



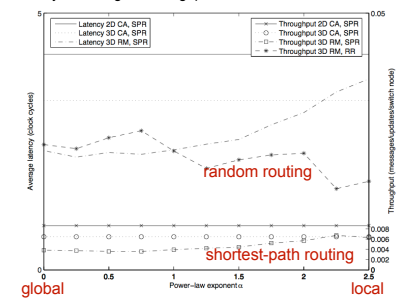
## Average path length and number of hops:

- With few global connections, the 3D random small-world topology has a lower average path length and lower number of hops.



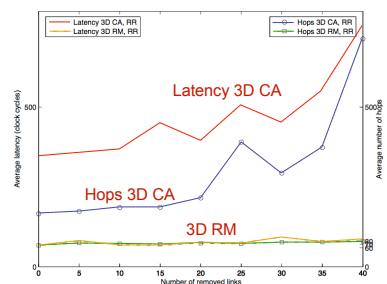
## Latency and throughput:

- The 3D random small-world topology offers a lower average latency and a higher throughput for random traffic.



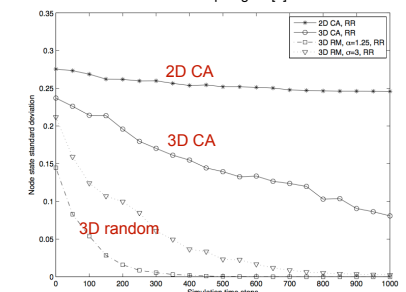
## Robustness against link removals:

- The small-world random network is more robust against random link removals than the regular 2D and 3D topologies.



## Solving the synchronization and density task:

- Synchronization is faster because of the better network transport characteristics of small-world topologies [8].



## Conclusions and future work:

- Small-world-like interconnects with a power-law distribution of the connections as a function of the Euclidian distance [4,5]:
  - are physically plausible (long distance connections are costly), and
  - offer great transport characteristics using minimal resources.
  - Related work with similar outcome: see [7,8]
- Regular 3D is better than regular 2D, irregular small-world 3D is better than regular 3D.
- Problems can be solved more efficiently because of the better transport characteristics of SM topologies.
- Programming such an assembly can be challenging!
- Future work:
  - Simple, localized, and realistic routing algorithms
  - More realistic traffic models
  - Realistic wire-growth models that address fabrication issues
  - Do arbitrary computations on a random assembly

## References:

- [1] C. Teuscher. **On Irregular Interconnect Fabrics for Self-Assembled Nanoscale Electronics**. 2nd IEEE International Workshop on Default and Fault Tolerant Nanoscale Architectures, NANOARCH'06, June 17, 2006, Boston, MA, USA. Pages 60-67. → [arXiv:cond-mat/0605584](https://arxiv.org/abs/cond-mat/0605584)
- [2] L. Benini and G. de Micheli. **Networks on chips: A new SoC paradigm**. IEEE Computer, 35(1):70-78, 2002.
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- [4] T. Petermann and P. De Los Rios. **Spatial small-world networks: A wiring-cost perspective**, 2005. → [arXiv:cond-mat/0501420](https://arxiv.org/abs/cond-mat/0501420)
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- [7] T. Y. Ogras and R. Marculescu. **"It's a Small World After All": NoC Performance Optimization Via Long-Range Link Insertion**. IEEE Transactions on VLSI, 14(7):693-706, 2006.
- [8] N. Oshida and S. Ihara. **Packet traffic analysis on scale-free networks for large-scale network-on-chip design**. Physical Review E, 74:026115, 2006.